Exhibit 11

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,579	10/21/2010	7619912	19473-0099RX1	3547

25224 7590 06/06/2016
MORRISON & FOERSTER, LLP
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EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/001,339	06/08/2010	7619912	043326-000-0021	5035

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PTOL-90A (Rev. 04/07)

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

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PTOL-90A (Rev. 04/07)

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORPORATION
Requester 1,

SMART MODULAR TECHNOLOGIES (WWH), INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

Appeal 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/001,579
Patent 7,619,912 B2
Technology Center 3900

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and JEREMY J. CURCURI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Requesters 1–3 made three separate requests for *inter partes* reexamination of U.S. Patent No. 7,619,912 B2 ("the '912 patent") issued to Jayesh R. Bhakta and Jeffrey C. Solomon, entitled *Memory Module Decoder*. The '912 patent issued November 17, 2009 and is assigned to Patent Owner, Netlist Inc. Requestor 1 requested reexamination of claims 1–51 of the '912 patent, which was assigned Control No. 95/001,339; Requester 2 requested reexamination of claims 1, 3, 4, 6–11, 15, 18–22, 24, 25, 27–29, 31–34, 36–39, 41–45, and 50 of the '912 patent, which was assigned Control No. 95/000,578; Requester 3 also requested reexamination of the same claims of the '912 patent as Requester 2, which was assigned Control No. 95/000,579. R1 Request 6; R2 Request 1; R3 Request 1.[1] On February 28, 2011, Control Nos. 95/001,339, 95/000,578 and 95/000,579 were merged into a single proceeding. Dec. *Sua Sponte* to Merge Reexamination Proc. 6.

Although indicating claims 1–136[2] are subject to reexamination in the RAN, the Examiner further states claims 44, 51, 55, 59, 64–66, 72–74, 76, 94–108, and

[1] Throughout this opinion, we refer to (1) the Appeal Briefs filed by Requester 1, Requester 2, Requester 3, and Owner as R1 App. Br., R2 App. Br., R3 App. Br., and PO App. Br. respectively; (2) the Respondent Briefs filed by Owner (for Requesters 1–3), Requester 1, Requester 2, and Requester 3 as PO-R1 Resp. Br., PO-R2 Resp. Br., PO-R3 Resp. Br., R1 Resp. Br., R2 Resp. Br., and R3 Resp. Br. respectively ; (3) the Rebuttal Briefs by Requester 1, Requester 2, Requester 3, and Owner as R1 Reb. Br., R2 Reb. Br., R3 Reb. Br., and PO Reb. Br.; (4) the Examiner's Answer (Ans.) mailed January 14, 2015; (5) the Examiner's Right of Appeal (RAN) mailed June 18, 2014, (6) the Action Closing Prosecution (ACP) mailed March 21, 2014, and (7) Requests for Reexaminations by Requester 1, Requester 2, and Requester 3 as R1 Request, R2 Request, and R3 Request respectively.

[2] Claims 52-136 were added during the course of reexamination. *See* RAN 4.

inherently teaches claim 16. R1 App. Br. 18 and R1 Reb. Br. 9 (citing 2d Wang Decl. ¶ 13 and Murdocca 248).

We agree that Amidi teaches using a command signal to read or write to a cell within a DDR memory device. *See* Amidi ¶ 61. Presumably, because Amidi discusses a particular cell within a bank, Requester 1 contends that the command signals are being transmitted to one DDR memory device at a time as recited. R1 App. Br. 18; R1 Reb. Br. 9. Yet, as the Examiner indicates:

> Requester 1 asserts that "[o]ne of ordinary skill in the art would have understood from the '152 publication [of Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned explanation to support the assertion. . . . . The claims require transmission of a command signal *to only one DDR memory device at a time*. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal *to only one DDR memory device at a time when there is a plurality of memory devices in a rank.*

RAN 29 (emphasis added).

That is, Figures 6A and 6B of Amidi show various command signals (e.g., CS0, CS1, CKE, CAS, RAS, and WE) being transmitted to more than one memory device. Amidi ¶ 62, Fig. 6A–6B (stating "Signals to Memory Devices" at the far right) Moreover, Amidi's Figures 6A and 6B undermines Requester 1's assertion that delivering command signals to two or more memory cells at a time would create data bus contention. *See* R1 Reb. Br. 9. That is, Amidi's Figures 6A and 6B further teach or suggest that the command signal is transmitted to a cell within *multiple* memory devices at a time. Thus, although Dr. Wang's testimony states that the RAS and CAS signals are used to isolate a particular memory cell in an array of a memory device (2d Wang Decl. ¶ 13), there is countering evidence in

Amidi to demonstrate that isolating a cell relates to isolating a cell within multiple memory devices at the same time.

Lastly, Murdocca does not form any part of the rejection based on Grounds 4 and 6. *See* R1 App. Br. 18. Even so, Murdocca's cell that is formed by an intersection of the row and column address does not refute Amidi's teaching that the command signals are transmitted to memory *devices*.

Accordingly, we are not persuaded that the Examiner erred in not adopting the rejection of claims 16 and 132, which has similar limitations, based on Amidi or Amidi and JEDEC.

Requester 1 provides arguments for dependent claims 17 and 133. R1 App. Br. 18–19. We will sustain the Examiner's decision not to reject these claims, because these claims depend from claim 16 and claim 132 respectively.

As for dependent claim 58, Requester 1 argues the rejection of this claim should be adopted based on its previous contention. R1 App. Br. 18. As discussed above, claim 57, from which claim 58 depends is not disputed. PO App. Br. 47. Claim 58 has similar limitations to claim 1. Thus, for the above reasons when addressing claim 1, we will sustain the Examiner's decision not to reject claim 58 based on Amidi.

Requester 1 further argues specifically that dependent claims 56 and 60 should be rejected based on Amidi and JEDEC (Ground 6). R1 App. Br. 25–26. These claims depend indirectly from claims 52 and 57 respectively. Because we agree that the Examiner did not err in not adopting the rejection of claims 52 and